UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,462	10/20/2003	Wen-Ting Chu	N1085-00156	4151

54657 7590 06/01/2007

DUANE MORRIS LLP
IP DEPARTMENT (TSMC)
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
06/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,462	CHU ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 34-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 34-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on March 19, 2007.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 39 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 6,524,915 B2).

In re claims 39, Kim et al. discloses (figs. 6A-6N) a method of forming a split gate field effect transistor, comprising: providing a substrate (200) comprising a pair of floating gates (202) and a first conductive material layer (209) between said pair of floating gate layers and spaced therefrom, and a first dielectric layer (216 on layer 209) above said first conductive material layer; forming a substantially rectangular control gate (214a) comprising a second dielectric layer (216 on layer 214a) above said control gate, wherein said control gate is self-aligned to said pair of floating gates by using said first and second dielectric layers as an etching hard mask (col. 8, lines 18-22); said control gate not overlaying said pair of floating gates.

In re claim 40, Kim et al. discloses (fig. 6N) forming a pair of source/drain regions (224) into said substrate and beside said pair of floating gates and said control gate

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,524,915 B2) in view of Wang (US 6,541,324 B1).

In re claims 1 and 36, Kim et al. discloses (figs. 6A-6N) a method of forming a split gate field effect transistor comprising: providing a substrate (200) having a pair of floating gate portions (formed from layer 202 in fig. 6A), a first conductive material layer (209) between the pair of floating gate layer portions, and a first dielectric layer (213) above said first conductive material layer; forming a pair of floating gates (211, fig. 6E) from said pair of floating gate layer portions; forming a substantially rectangular control gate (218, fig. 6K) having a second dielectric layer (216) above said control gate, wherein said control gate is self-aligned to said pair of floating gates by using said second dielectric layer as a second etching hard mask (col. 8, lines 18-22); the control gate does not overlay the pair of floating gates; and forming a pair of source/drain regions (224) into the substrate and beside the pair of floating gates and said control gate. Kim shows all of the elements of the claims except forming the floating gates

using the first dielectric layer and the control gate being formed using the first and second dielectric layers as a second etching hard mask. Wang shows (figs. 3H-3P) that a first dielectric layer (58) is used as an etch mask to form the floating gates (14, fig. 3J) and that the first dielectric layer (58) and the second dielectric layer (142) is used as an etch mask to form the control gates (144, fig. 3P). With this process modification, the memory device is formed by using a low number of masking steps (col. 13, lines 60-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of forming the floating gates and control gates of Kim by using the first and second dielectric layers a mask layer as taught by Wang to reduce the number of masking steps in the formation process.

In re claims 2-4, 34, and 35 Kim discloses (col. 7, lines 59-65 and col. 8, lines 11-14) that the first (213) and second dielectric (216) layers comprise a silicon oxide layer. The second dielectric layer is formed by thermal oxidation. Neither reference discloses the thickness of the oxide layer. However, it would have been obvious to one of ordinary skill in the art to make the oxide layer within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

In re claim 5, Kim shows (fig. 6I) that a second dielectric layer (216) formed on the control gate portion (214a) is thicker in the middle than at an edge portion.

In re claims 6-8 and 37, Wang discloses (figs. 3M-3P) that the step of forming the control gate comprises: forming a second conductive material layer (66) above the substrate; forming a hard mask layer (134) above said second conductive material layer; removing portions of said hard mask layer and said second conductive material layer (fig. 3O); and removing a remaining portion of said hard mask layer and an additional portion of said conductive material layer (fig. 3P) by using said first dielectric layer (58) and said second dielectric layer (142) as said second etching hard mask. The second dielectric layer (142) is formed by using said hard mask layer as an oxidation resistant layer, and the hard mask layer comprises silicon nitride (col. 10, line 42 - col. 11, line 11).

Claims 9-13 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,524,915 B2) in view of Wang (US 6,541,324 B1) as applied to claims 1 and 36 above, and further in view of Ryu et al. (US 6,800,525 B2).

In re claims 9-13 and 38, Kim in view of Wang shows all of the elements of the claims except the step of removing portions of the hard mask layer and second conductive material layer comprising forming a sacrificial layer. Ryu discloses (fig. 2g) that a sacrificial layer (216) is formed above the hard mask layer (215) . The method also includes removing portions of the sacrificial layer (216), the hard mask layer (215) and the second conductive layer (214) (fig. 2h). A remaining portion of the sacrificial layer is also removed (fig. 2k). By forming a sacrificial layer over the substrate, step coverage throughout the entire substrate is improved during the planarization process

(col. 5, lines 1-13). The sacrificial layer (216) is used to planarize the surface of the substrate (fig. 2i). The sacrificial layer may be an HDP-CVD film (organic), which may function as a photoresist, or a USG (spin on glass) layer (col. 5, lines 9-12). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Kim and Wang by adding a sacrificial layer as taught by Ryu to improve the step coverage across the entire substrate during a planarization process.

Response to Arguments

Applicant's arguments with respect to claims 1-13 and 34-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren
May 29, 2007